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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
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Toyohiko YOSHIDA et al.	)	Group Art Unit: 2183
	)	
Application No.: 09/146,259	)	Examiner: W. Treat
	)	
Filed: September 3, 1998	)	Appeal No.
	)	
For: DATA PROCESSING DEVICE	)	
	)	
	)	
	)	

BRIEF FOR APPELLANT

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: April 4, 2002

Sir:

This appeal is from the decision of the Primary Examiner dated September 6, 2001 (Paper No. 15), in which claims 1-25 were finally rejected. A copy of claims 1-25 is reproduced in an Appendix to this brief.

A check covering the [ ] $160.00 (220) [X] $320.00 (120) Government fee and two extra copies of this brief are being filed herewith.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in triplicate.

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I. Real Party of Interest

The present application is assigned to Mitsubishi Denki Kabushiki Kaisha, who is the real party of interest.

II. Related Appeals and Interferences

There are no known currently pending related appeals or interferences in the subject application.

III. Status of Claims

Claims 1-25 remain pending in the subject application.

IV. Status of Amendments

A response to the final Office Action was filed on November 9, 2001. No claim amendments were made in the November 9, 2001 response. In the Advisory Action dated November 29, 2001, the Examiner stated that "Applicants' arguments did not overcome his §112 or drawing problems. In view of the lack of clarity, the art rejection stands."

V. Summary of the Invention

The present invention relates to a data processing device for properly scheduling conditional operation instructions in a program sequence. (page 1, lines 5-7)

Figure 1 is a block chart for showing a constitution of a microprocessor according to Embodiment 1 of the present invention. This microprocessor is a 32-bit microprocessor

having an internal data bus of 32 bits. In this Figure, reference numeral 2 designates an instruction decode unit (instruction decoder) for performing a process of decoding an instruction code inputted from an instruction RAM 6 through an ID bus having a width of 64 bits; reference numeral 3 designates a memory unit (instruction execution unit) for performing an address calculation; reference numeral 4 designates an integer operation unit (instruction execution unit) for performing an arithmetic logic operation and/or a shift operation; reference numeral 5 designates a general purpose register of 32 bits × 64 words; and reference numeral 7 designates a data RAM for storing data. (page 17, line 17 through page 18, line 6)

Figures 2a and 2b are views for explaining instruction formats of the microprocessor 1. In the instruction formats, there are included a format 101 of dual operation instruction which designates two operations by one instruction word as shown in Figure 2a and a format 102 of single operation instruction which designates one operation by one instruction word as shown in Figure 2b. (page 21, line 26 through page 22, line 6)

In the format 101 of dual operation instruction, there is included a format field composed of a field 103 and a field 104, two operation fields 106 and 107, execution condition fields 401 and 402 respectively attached to the operation fields 106 and 107, and fields for designating amount of delay for judging condition (hereinbelow, referred to as CD field) 404 and 405 respectively attached to the execution condition fields 401 and 402. (page 22, lines 7-15)

The format 102 of single instruction operation 102 includes a format field composed of fields 103 and 104, an operation field composed of fields 108, 109, and 110, an

execution condition field 403 attached to the operation field and a CD field 406 attached to the execution condition field 403. (page 22, lines 16-21)

A plurality of pipeline stages in the microprocessor 1 are formed of an instruction fetch stage IF, an instruction decode stage D/A, an instruction execution stage E/M and a write back stage W, wherein processings in each stage are finished within one clock cycle. Figure 3a through 3c are schematic views for explaining the pipeline stages for processing the dual operation instruction 101 in the microprocessor 1. In the instruction fetch unit IF, the dual operation instruction 101 is fetched from a memory RAM 6 to an instruction decode unit 2. In the instruction decode stage D/A, operation_0 described in the operation field 106 is decoded by the decoder 8 and operation_1 described in the operation field 107 is decoded by the decoder 9. Further, addresses of each operand of operation_0 and operation_1 or, in a case that operation_0 and operation_1 are branch sub-instructions, addresses of destination of branch are calculated in the instruction decode stage D/A. In the instruction execution stage E/M, an operation designated by operation_0 in accordance with a control signal 11 is executed in the memory unit 3, and an operation designated by operation_1 in accordance with a control signal 12 is executed in the integer operation unit 4. When operation_1 is a sub-instruction accompanying memory access such as a load sub-instruction and a store sub-instruction, the memory unit 3 accesses to the memory in the instruction execution stage E/M. In the write back stage W, a result of operation obtained in the memory unit 3 and a result of operation obtained in the integer operation unit 4 are written in registers designated by operation_0 and operation_1 respectively. In a sub-instruction which does not accompany a sub-instruction of writing a result of operation in a

register of the processor 1, namely, a branch sub-instruction, a jump sub-instruction, a store sub-instruction storing a memory with data, a comparison sub-instruction reflecting a result of operation in a flag and so on, a write back stage W is not included. Depending on a microprocessor, a write back stage W is processed in the same clock cycle as that of an instruction execution stage E/M. (page 23, line 6 through page 24, line 20)

In the case of FM=00, the stages IF, D/A, E/M, and W respectively of operation_0 and operation_1 are performed in parallel, and operation_0 and operation-1 are processed in 4 clocks, as shown in Figure 3a. (page 24, lines 21-24)

In the case of FM=01, the stages IF, D/A, E/M and W of operation_0 are continuously performed in 4 clocks, as shown in Figure 3b. The stages IF and D/A respectively of operation_0 and operation_1 are performed in parallel. Meanwhile, the stages E/M and W of operation_1 are performed with a delay of 1 clock from those of operation_0. The stage E/M of operation_1 is performed in parallel with the stage W of operation_0. Accordingly, operation_1 is processed in 5 clocks. In the case of FM=01, the stages IF, D/A, E/M and W are continuously performed in 4 clocks, as shown in Figure 3c. The stages IF and D/A respectively of operation_0 and operation_1 are performed in parallel. Meanwhile, the stages E/M and W of operation_1 are performed with a delay of 1 clock from those of operation_1. The stage E/M of operation_0 is performed in parallel with the stage W of operation_1. Accordingly, operation_1 is processed in 5 clocks. (page 24, line 25 through page 25, line 14)

Also, a single operation instruction 102 having a format shown in Figure 2b is also processed in 1 clock cycle in each of the instruction fetch stage IF, the instruction decode

stage D/A, the instruction execution stage E/M and the write back stage W. In the stage IF, the single operation instruction 102 is fetched from the instruction RAM 6 to the instruction decode unit 2. In the stage D/A, the single operation instruction 102 is inputted respectively in the decoders 8 and 9. In response to a type of operation designated by the single operation instruction 102, one of the decoders 8 and 9 decodes the single operation instruction 102. When the decoder 8 decodes, it outputs a control signal 11, and when the decoder 9 decodes, it outputs a control signal 12. In the stage E/M, the memory unit 3 (or the integer operation unit 4) executes the operation designated by the single operation instruction 102 in accordance with the control signal 11 (or the control signal 12). In the stage W, a result of operation obtained in the stage E/M is written in a register designated by the single operation instruction 102. (page 25, line 16 through page 26, line 9)

Next, the CD field in the instruction formats shown in Figures 2a and 2b will be described in detail. The CD field 404 is to designate an amount of delay by which timing of judging an execution condition designated by the execution condition field 401 corresponding thereto in a pipeline process of operation_0 designated by the operation field 106 corresponding thereto, wherein the amount of delay can be variably set when a user sets a value of CD field 404 appropriately. (page 39, line 25 through page 40, line 7)

Specifically, in the CD field 404, an offset value OVA from a memory address X of the instruction with the format 101 is described as an immediate value. In this case, timing of judging the execution condition described in the execution condition field 401 in the process of operation_0 is a clock cycle when a PC value of the microprocessor holds the address No. (X+OVA), wherein the offset value OVA can be 0. In such a case, the timing

of judging the execution condition is a clock cycle when the PC value holds the address No. X. Further, it is possible to describe a description designating a register number of a register in the processor 1 which holds an address value in the CD-field 404. In this case, the timing of judging the execution condition described in the execution condition field 401 is a clock cycle where the PC value of the microprocessor 1 is an address held in the designated register. A bit for distinguishing whether an immediate value is described in the CD field 404 or a register number is described therein exists in the identical CD field 404. (page 40, line 8 through page 41, line 1)

However, when the execution condition field 401 designates the unconditional execution of CC=000, the value of CD field 404 is ignored by the instruction decode unit 2 and the units 3 and 4 at the process of executing operation_0 corresponding thereto. (page 41, lines 2-6)

The CD field 405 works the same as the CD field 404 does with respect to the operation field 107 and the condition execution field 402. Further, the CD field 406 works the same as the CD field 404 does with respect to operations of the fields 108 through 110 and the conditional execution field 403. (page 41, lines 7-12)

Registers in the memory unit 3 shown in Fig. 1 will be described. (page 41, lines 13-14)

The register 32 in the PC controlling part 13, the register 42 in the memory controlling part 14, the register 52 in the ALU 15 and the register 62 in the shifter 16 hold a description of a time for judging the execution condition of the operation_0. (page 42, lines 2-6)

In a case a single operation instruction is processed by the instruction format 102, one of the PC controlling part 13, the memory controlling part 14, ALU 15, ALU 19, the shifter 16, the shifter 20 and the multiplier 17 executes an operation sub-instruction as an operation unit of the instruction execution unit depending on a type of operation such as a branch, a memory access and an arithmetic operation. The CD field 406 designates an amount of delay by which a time for judging an execution condition designated by the execution condition field 403 similarly in a pipeline process of a single operation instruction. Further, a register provided in the operation unit of the instruction execution unit for executing the single operation instruction 102 holds a value having the same content as described about the single operation instruction 102 in the above. (page 49, line 12 through page 50, line 1)

In the next, the operation of the microprocessor 1 will be described with reference to an example of a program shown in Figure 8. (page 50, lines 2-4)

In this program, a pair of sub-instructions in each row is described by a dual operation instruction 101 having the instruction format shown in Figure 2a, wherein sub-instructions I01, I11, I21, I31, I41, I51 and I61 are described in the operation field 106 as operation_0, and sub-instructions I02, I12, I22, I32, I42, I52, and I62 are described in the operation field 107 as operation_1. Each dual operation instruction is accessed by means of an address number of memory described in the identical row. For example, the sub-instructions I01 and I02 are stored in a memory area of No. 1000 through No. 1007 and accessible at an address No. 1000. (page 50, lines 5-17)

The sub-instruction I01 is a branch instruction BRA for taking a branch to sub-instruction I11 and I12 having a description of "loop" when a branch condition that "flag F0 is false (namely, flag F0 holds 0) is satisfied, wherein the branch condition is judged at the time of executing the sub-instruction I41 and I42. And the branch instruction BRA is an ordinary branch instruction without delay. The sub-instruction I21 is an add instruction ADD which adds a content of a register R2 to a content of a register R3 and stores the result of addition register R2. The sub-instruction I31 is a comparison instruction CMPEQ which writes "1" in the flag F0 when the content of register R2 and a content of register R4 are equal and "0" therein when the contents are not equal. The sub-instructions I11, I41, I51, and I61 are arbitrary arithmetic operation instructions by which the stage E/M is processed in the memory unit 2, and other sub-instructions are arbitrary arithmetic operation instructions by which the stage E/M is processed in the integer operation unit 3. (page 50, line 18 through page 51, line 10)

Figure 9 shows operation of the microprocessor 1 which processes the program shown in Figure 8 in pipeline. In the Figure, clocks t1 through t13 designate continuous one clock cycles, and all pipeline stages in each clock cycle are processes in parallel. For example, in clock t5, each stage W in the sub-instructions I11 and I12, each stage E/M in the sub-instructions I21 and I22, each stage D/A in the sub-instructions I31 and I32 and each stage IF in the sub-instructions I41 and dI42 are processed in parallel respectively. Stages in other clock cycles are similarly processes thereto. (page 52, lines 2-12)

In Figure 9, an address value held by the PC of microprocessor 1 shows that the clock cycle corresponding to the address value is a cycle just after the cycle of processing

the dual operation instruction which is accessed by the address value on the instruction decode stage D/A. (page 52, lines 13-18)

Concerning the sub-instructions I01 and I02, the instruction fetch stage IF, and the instruction decode stage D/A are processed in parallel respectively in the clock t1 and the clock t2. Although the instruction execution stage E/M and the write back stage W of the sub-instruction I02 are processed respectively in the clocks t3 and t4, the instruction execution stage E/M of the sub-instruction I01 is not processed by judging the execution condition and branching based on this judgment, until it is enabled to process. (page 52, line 19 through page 53, line 1)

The instruction decode unit 2 detects that the sub-instruction I01 is a sub-instruction for delaying judgement of execution condition in accordance with the field for designating condition 401 and the CD field 404 both of which are of the branch sub-instruction BRA as the sub-instruction I01, and the contents of the field for designating condition and the CD field are outputted to the PC controlling part as a control signal for judging the execution condition with a delay. Also, the field for designating operation is decoded in the decoder 8 and a control signal 11 is outputted in response to the result of decoding. In the control signal 11, a first description for controlling the PC controlling part 13 so as to take a branch of the branch sub-instruction BRA, a second description for showing that the sub-instruction I01 is an ordinary sub-instruction which does not cause a delay of execution, a third description for indicating a branch address of the branch sub-instruction BRA are included. The third description is the branch address itself, which is calculated by an adder for exclusively calculating address (not shown) based on an offset designated by the field

323 of the branch sub-instruction BRA at the instruction decode stage E/A. (page 53, lines 2-25)

In the clock t3, the PC controlling part 13 receives a description that the sub-instruction I01 from the instruction decode unit 2 is a conditional sub-instruction and a sub-instruction for delaying a time of judging the condition, and holds the control signal 11 with respect to the branch sub-instruction BRA in its register 30 without change. At this time, the branch is not executed based on the control signal 11. A value of CC=010 which is the execution condition field outputted from the instruction decode unit 2 is held in the register 31 without change. Further, the PC controlling part 13 receives an offset value "20" which is the CD field from the instruction decode unit 2 and the address No. 1000 from the PC, adds these, and holds a result of the addition of the address No. 1020 in its register 32 at the clock t3. The PC controlling part 13 is comparing the value held in the register 32 with the value indicated by the PC. The PC controlling part 13 judges the execution condition of the branch sub-instruction BRA based on a clock cycle at which the address value in the PC is equal to the address value in the register 32, namely, a CC value held in the register 31 at the clock t7. (page 53, line 26 through page 54, line 21)

On the other hand, the decoder 9 of the instruction decode unit 2 analyzes the field for designating operation 107 to thereby output a control signal 12 for commanding ALU 18 to perform an arithmetic operation, with respect to the sub-instruction I02. The instruction decode unit 2 detects, based on the field for designating condition, that the sub-instruction I02 is an unconditional sub-instruction, and outputs a description of showing

that the sub-instruction I02 is unconditional (CC=000). (page 54, line 22 through page 55, line 4)

ALU 18 performs an add operation in accordance with a control signal 12 without holding the control signal 12 in its register 80 when the description that it is unconditional is received. Further, the value of execution condition field 402 and the value of CD field 405 both in the sub-instruction I01 are outputted from the instruction decode unit 2. However, ALU 18 holds values already held in the registers 81 and 82 without change by ignoring the value of execution condition field 402 and the value of CD field 405. As for other sub-instructions to be executed unconditionally, the similar processes thereto are applicable. (page 55, lines 5-17)

The branch condition of the branch sub-instruction BRA is judged at the clock t7 because a result of operation by the sub-instruction I31 should be referred to. At the clock t7, the PC controlling part 13 refers to the flag F0 in accordance with the value '010' held in the register 31, determines to take a branch when the flag F0 is '0', and determines not to take a branch when the flag F0 is '1'. (page 57, lines 6-13)

The PC controlling part 13 ignores a content of the register 33 in accordance with an event that the second description of the control signal 11 held in the register 30 shows that the branch sub-instruction BRA is a branch sub-instruction without delay. In other words, the instruction execution stage E/M is processed at the same clock t7 in accordance with an event that the branch condition is determined in the PC controlling part 13. Since the sub-instruction I41 is an arithmetic operation sub-instruction and the instruction execution stage E/M therefore is processed in ALU 15 not in the PC controlling part 13,

the stages E/M of the sub-instruction I01 and the sub-instruction I41 can be processed in parallel. (page 57, lines 14-27)

Needless to say, as for the delayed jump sub-instruction DJMP or the delayed branch sub-instruction DBRA, it is possible to execute a branch at the same cycle as the clock cycle at which the execution condition is judge by changing a value of the field for designating amount of execution delay 322. (page 70, line 26 through page 71, line 2)

It is not limited to a conditional branch or a jump sub-instruction to delay a time for judging an execution condition. It is possible to delay a time for judging execution conditions designated by the fields for designating condition 401 through 403 by the CD formats 404 through 406 in execution processings of two arbitrary sub-instructions of a dual operation instruction and of an arbitrary single operation instruction 102. (page 71, lines 2-11)

VI. The Issues

The issues presented for review are:

a) whether claims 1-25 were properly rejected under 35 U.S.C. §112, first paragraph and whether the drawings were properly objected to under 37 C.F.R. § 1.83(a);

b) whether claims 1-25 were properly rejected under 35 U.S.C. §102(e) or, in the alternative, under 35 U.S.C. §103 as obvious over *Holmann et al* (U.S. Patent No. 5,815,698).

VII. Grouping of Claims

Applicants respectfully submit that claims 2-13, 15-20 and 22-25 do not stand and fall together with claims 1, 14 and 21, since it is respectfully submitted that claims 2-13, 15-20 and 22-25 are separately patentable as discussed below.

VIII. Applicants' Arguments Against the Rejection of the Claims Under 35 U.S.C. §112, First Paragraph and Objection to the Drawings

A. Errors in the rejection/objection

It is respectfully submitted that the rejection of claims 1-25 under 35 U.S.C. §112, first paragraph and objection to the drawings is erroneous because the specification and drawings as originally filed provide support for the invention as now claimed.

B. How the first paragraph of 35 U.S.C. §112 and 37 C.F.R. § 1.83(a) are complied with

Applicants respectfully traverse the rejection of claims 1-25 under 35 U.S.C. §112, first paragraph, and in particular the Examiner's statement that "Applicants' claim mix the capabilities of instructions and sub-instructions without distinguishing as to what provides the capabilities and implying applicants have some form of hybridized instructions which are not enabled." Applicants respectfully bring the Board's attention to Figures 2a and 2b. Figure 2a clearly shows a dual operation instruction which designates two operations by one instruction word, while Figure 2b shows a single instruction operation which designates one operation by one instruction word. (see specification page 21, line 26 through page 22, line 6) While Applicants admit that the two operation fields of the dual operation

instruction are referred to as sub-instructions, Applicants respectfully submit that both Fig. 2a and 2b represent one instruction word. Thus, the instruction decoder decodes a plurality of instructions (i.e. instruction words) regardless of whether they are dual operation instruction or a single operation instruction. Applicants respectfully submit that their invention is not limited to the dual operation instruction having two operations (i.e. sub-instructions) but also includes the single operation instruction. Applicants also respectfully bring the Board's attention to page 25, line 16 through page 26, line 9 of the specification, which describes the processing of a single operation instruction. Applicants respectfully submit that the claims are written to encompass both the dual operation instruction and the single operation instruction. Therefore, applicants respectfully traverse the Examiner's rejection of claims 1-25 under 35 U.S.C. §112, first paragraph, since limiting the claims to the format of the dual operation instruction only, as suggested by the Examiner, is improper and not supported by the description in the specification.

Furthermore, Applicants respectfully that PC control part 13 in Fig. 1 contains registers 30-33. Furthermore, Figures 8 and 9 as well as the description in the specification corresponding thereto describes the specific sequence of events and timing relationships corresponding to one example of dual operation instructions. However, examples using the dual operation instruction do not preclude single operation instructions. Applicants respectfully bring the Board's attention to page 71, lines 10-11. Thus, while applicants provide several examples using dual operation instruction shown in Figure 2a, applicants' invention is not limited thereto. Applicants respectfully submit that the specification and drawings provide support for the invention as claimed in claims 1-25. It is therefore

respectfully requested that the Board reverses the Examiner's objection to the drawings and rejection of claims 1-25 under 35 U.S.C. §112, first paragraph, since it is respectfully submitted that the specification and drawings as originally filed provide support for the invention as now claimed.

IX. Applicants' Arguments Against the Rejection of Claims 1-25 Under 35 U.S.C. §102(e)

A. Errors in the rejection

It is respectfully submitted that the rejection of claims 1-25 under 35 U.S.C. §102(e) is erroneous because the prior art does not show, teach or suggest a) decoding an instruction in a second period and determining an execution condition in a fourth period as claimed in claim 1, b) a register storing a value representing a timing of starting to determine an execution condition as claimed in claim 14, or c) a field specifying a time to start a determination of whether a condition is satisfied as claimed in claim 21.

B. Explanation of why the claims are patentable under 35 U.S.C. §102(e)

Holmann et al appears to disclose a microprocessor which can execute a delayed jump instruction. When the instruction decoder 8 in the instruction decode unit 8 recognizes that a decoded instruction is a delayed branch instruction, the instruction decoder unit 2 generates a control signal 11 and transfers it to the memory unit 3. In the memory unit 3, the PC controller 13 stores the decoded instruction into register 13A according to the control signal 11 received from the instruction decoder unit 2. Accordingly, the register 13A stores information indicating the target of a delayed branch instruction. The PC

controller 13 stores a PC value related to the time when the branch instruction will be executed into register 13B. When the value of the program counter (PC) in the microprocessor is equal to the value stored in register 13B, the PC controller 13 executes the branch instruction based on the target branch information stored in register 13A. That is, the value designated by the target branch information stored in register 13A is set into the program counter (PC). As a result, when the address of a fetched instructions is equal to the value stored in register 13B, the instruction at the target of a branch is fetched in the following cycles. (col. 14, lines 26-45)

Thus, *Holmann et al* merely discloses executing a delayed jump instruction. However, as claimed in claims 1, 14 and 21, the claimed invention is directed to executing a conditional instruction. In other words, in the present invention, a branch is not executed until a certain condition is satisfied. In particular, as claimed in claims 1, 14 and 21, the timing of determining the condition is delayed. In particular, as claimed in claim 1, the instruction is decoded in a second period and the execution condition is determined in a fourth period which is started after a certain duration therefrom. Claim 14 claims a first register for holding a first description indicating a timing for starting a determination of the condition. Claim 21 claims a field specifying a timing of starting a determination whether a condition is satisfied. Nothing in *Holmann et al* shows, teaches or suggests delaying of a timing of determining a condition. Rather, *Holmann et al* merely discloses executing of the instruction is delayed. However, an execution condition is not determined in *Holmann et al.* and the timing of determining the condition is not delayed in *Holmann et al.*

Additionally, nothing in *Holmann et al* shows, teaches or suggests an instruction execution unit starts the judgment of whether or not the second operation instruction satisfies the predetermined condition in response to a value held in a register for designating amount of delay as claimed in claim 2. Furthermore, nothing in *Holmann et al* shows, teaches or suggests the second instruction has a field for designating operation and a field for designating amount of delay which designates an interval between the ending of the third period and the starting of the fourth period as claimed in claim 3. Furthermore, nothing in *Holmann et al* shows, teaches or suggests the instruction execution unit starts the judgment of whether or not the second instruction satisfies the predetermined condition in response to an event that an address value held in a register is in agreement with a value of a program counter as claimed in claim 4.

Additionally, nothing in *Holmann et al* shows, teaches or suggests an instruction execution unit determines whether or not the predetermined condition is satisfied in a fifth period and executes the operation designated by the second instruction in a sixth period when the predetermined condition is satisfied, as claimed in claim 5. Furthermore, nothing in *Holmann et al* shows, teaches or suggests an instruction execution unit starts the judgment of whether or not the second instruction satisfies the predetermined condition in accordance with a value held in a first register and starts to execute the operation designated by the second instruction when the predetermined condition of the second instruction is satisfied in accordance with a value held in a second register as claimed in claim 6. *Holmann et al* also does not disclose the fields of the second instruction as claimed in claim 7 or the instruction unit starts to judge whether or not the predetermined condition is

satisfied in response to an event that an address value is in agreement with a value of a program counter and starts to execute the operation designated by the second operation instruction when the predetermined condition is satisfied in response to an event that the address value is in agreement with the value of the program counter as claimed in claim 8.

Also, nothing in *Holmann et al* shows, teaches or suggests an instruction decoder decodes a third instruction in a seventh period which is started after the third period in order to output a third control signal, and the instruction execution unit executes an operation designated by the third instruction and writes a result in an eighth period as claimed in claim 9. Additionally, nothing in *Holmann et al* shows, teaches or suggests the third instruction is a comparison instruction which compares values of two registers and writes a result of the comparison in a predetermined memory location as claimed in claim 10. Furthermore, nothing in *Holmann et al* shows, teaches or suggests the second instruction is a branch instruction, a jump instruction or an add instruction as claimed in claim 11, or that each of the plurality of instructions has a plurality of fields and that the instruction decoder outputs a second control signal and controls the instruction execution unit to determine whether or not the condition is satisfied in a fourth period as claimed in claim 12. Also, nothing in *Holmann et al* shows, teaches or suggests that each of the plurality of instructions has a plurality of fields and that the first instruction is a conditional instruction as claimed in claim 13.

Also, nothing in *Holmann et al* shows, teaches or suggests the first description held in the first register could be variably set as claimed in claim 15 or further comprising a program counter and that the instruction execution unit starts to determine whether or not a

condition is satisfied in response to a detection that the address value held in the first register is in agreement with an address of the program counter as claimed in claim 16. Also, nothing in *Holmann et al* shows, teaches or suggests a conditional instruction has a plurality of fields and the instruction execution unit writes in the first register based on a field output by the decoder as claimed in claim 17. Also, nothing in *Holmann et al* shows, teaches or suggests the instruction execution unit detects timing for starting the operation designated by the instruction, determines whether or not the condition is satisfied and starts the operation in response to the result of the determination as claimed in claim 18.

Also, nothing in *Holmann et al* shows, teaches or suggests the instruction execution unit detects an event that the address held in the first register is in agreement with the address of a program counter, starts to determine whether or not the condition is satisfied in response to the detection, detects an event that the address held in the second register is in agreement with the address of the program counter and starts to execute the operation designated by the instruction in response to the detection as claimed in claim 19. Also, nothing in *Holmann et al* shows, teaches or suggests the conditional instruction has a plurality of fields and that the instruction execution unit performs a determination based on a third description held in a fourth register, reads the first control signal from the third register in response to the result of the determination and executes the operation in accordance with the first control signal read from a third register as claimed in claim 20.

Also, nothing in *Holmann et al* shows, teaches or suggests a program counter or an instruction execution unit which includes a register into which a program counter value is written and starts a determination when detecting a coincidence of the program counter

value with the address of the program counter claimed in claim 22. Furthermore, nothing in *Holmann et al* shows, teaches or suggests the condition instruction includes another field specifying a time of starting the operation as claimed in claim 23. Also, nothing in *Holmann et al* shows, teaches or suggests the condition instruction includes another field specifying a timing of starting the operation as claimed in claim 24 or that the execution unit further includes a second register for holding a first control signal and a third register for holding a second description indicating the condition as claimed in claim 25.

Since nothing in *Holmann et al* shows, teaches or suggests a) decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1, b) a register storing a value representing a timing of starting to determine an execution condition as claimed in claim 14, or c) a field specifying a timing to start a determination of whether a condition is satisfied as claimed in claim 21 or any of the other features as claimed in claims 2-13, 15-20 and 22-25, it is respectfully submitted that *Holmann et al* does not anticipate the invention as claimed in claims 1-25. Therefore, it is respectfully requested that the rejection of claims 1-25 under 35 U.S.C. §102(e) be reversed.

X. Applicants' Arguments Against the Rejection of Claims 1-25 Under 35 U.S.C. §103

A. Errors in the rejection

It is respectfully submitted that the rejection of claims 1, 14 and 21 is erroneous because the difference between the present invention and the prior art relied upon by the

Examiner is such that the invention would not have been obvious to a person having ordinary skill in the art at the time the invention was made.

B. Limitations not described in the prior art

The limitations not described in the prior art are:

1) decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1;

2) a register storing a value representing a timing of starting to determine an execution condition as claimed in claim 14; or

3) a field specifying a timing to start a determination of whether a condition is satisfied as claimed in claim 21.

C. Explanation of why the limitations render the claimed subject matter allowable over the prior art

As discussed above, *Holmann et al* merely discloses designating a timing of executing a branch. Nothing in *Holmann et al* shows, teaches or suggests a conditional instruction and in particular *Holmann et al* does not show, teach or suggest delaying a timing of determining the condition as claimed in claims 1, 14 and 21. Rather, *Holmann et al* only discloses delaying executing the instruction to a designated timing.

In other words, nothing in *Holmann et al* shows, teaches or suggests decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1, a register

storing a value representing a timing of starting to determine an execution condition as claimed in claim 14 or a field specifying a timing to start a determination of whether a condition is satisfied as claimed in claim 21. Additionally, nothing in *Holmann et al* discloses the other features discussed above with respect to claims 2-13, 15-20 and 22-25 and not repeated here to avoid redundancy.

D. Why the reference taken as a whole does not suggest the claimed invention

As discussed above, nothing in *Holmann et al* shows, teaches or suggests delaying the timing of determining when a certain condition is satisfied as claimed in claims 1, 14 and 21. Furthermore, since *Holmann et al* is directed to a delayed branch instruction and not a conditional instruction, the determination of a delayed condition and the delaying thereof is not shown, taught or suggested by *Holmann et al*. Furthermore, none of the other features as claimed in claims 2-13, 15-20 and 22-25 as discussed above are shown, taught or suggested by *Holmann et al*. Therefore, it is respectfully requested that the Board withdraws the rejection to claims 1-25 under 35 U.S.C. §103.

XI. Conclusions

For all the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case since it is respectfully submitted that the final rejection of claims 1-25 is in error.

In the event this paper is not timely filed, Applicants petition for appropriate extension of time. Fees for this extension may be charged to our deposit account along with any other fees which may be required with respect to this application.

Respectfully submitted,

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APPENDIX A

The Appealed Claims

1. A data processing device comprising:

an instruction decoder for sequentially decoding a plurality of instructions described in a program sequence and outputting control signals respectively corresponding to the instructions, and

an instruction execution unit for executing operations respectively designated by said plurality of instructions in accordance with said control signal output from said instruction decoder, wherein

said instruction decoder decodes a first instruction among said plurality of instructions and outputs a first control signal in a first period;

said instruction execution unit executes the operation designated by said first instruction in accordance with said first control signal in a second period succeeding to said first period;

said instruction decoder outputs a second control signal in a third period by decoding a second instruction of which operation is executed under a predetermined condition among said plurality of instructions; and

said instruction execution unit determines whether or not said predetermined condition is satisfied in a fourth period and executes the operation designated by said second instruction in response to a result of the determination, said fourth period being started after elapsing a same time as said second period or longer from an ending of said third period.

2. A data processing device according to Claim 1 further comprising:

a register for designating amount of delay which can variably set a value to be held therein, wherein,

said instruction execution unit starts the judgement of whether or not said second operation instruction satisfies the predetermined condition in response to the value held in the register for designating amount of delay as an amount of delay.

3. A data processing device according to Claim 2, wherein

said second instruction has a field for designating operation and a field for designating amount of delay, which designates an interval between the ending of said third period and the starting of said fourth period; and the amount of delay is set in the register for designating amount of delay in accordance with a content described in said field for designating amount of delay.

4. A data processing device according to Claim 2 further comprising:

a program counter for sequentially counting addresses respectively corresponding to the plurality of instructions and holding the addresses, wherein

said register for designating amount of delay hold an address value to designate the amount of delay; and

the instruction execution unit starts the judgement of whether or not said second instruction satisfies the predetermined condition in response to an event that the address value held in said register for designating amount of delay is in agreement with a value of the program counter.

5. A data processing device according to Claim 1, wherein

the instruction execution unit determines whether or not the predetermined condition is satisfied in a fifth period included in said fourth period and executes the operation designated by said second instruction in a sixth period when said predetermined condition is satisfied, said sixth period being included in said fourth period and starting after elapsing the same time as said second period or longer from an ending of said fifth period.

6. A data processing device according to Claim 5 further comprising:

a first register for designating amount of delay and a second register for designating amount of delay both of which can variably set values to be held respectively therein, wherein

said instruction execution unit starts the judgement of whether or not said second instruction satisfies the predetermined condition in accordance with a value held in said first register for designating amount of delay as an amount of a first delay and starts to execute the operation designated by said second instruction when the predetermined condition of said second instruction is satisfied in accordance with a value held in said second register for designating amount of delay as an amount of a second delay.

7. A data processing device according to Claim 6, wherein

said second instruction has a field for designating operation, a field for designating amount of first delay which designates a time between the ending of said third period and

the starting of said fourth period and a field for designating amount of second delay which designates a time between the ending of said fifth period and the starting of said sixth period; and

the amount of said first delay is set in said first register for designating amount of delay in accordance with a content described in said field for designating amount of first delay and the amount of said second delay is set in said second register for designating amount of delay in accordance with a content described in said field for designating amount of said second delay.

8. A data processing device according to Claim 6 further comprising:

a program counter which sequentially counts addresses respectively corresponding to the plurality of instructions and holds the addresses, wherein

said first register for designating amount of delay and said second register for designating amount of delay hold address values respectively as the amount of said first delay and the amount of said second delay;

said instruction execution unit starts to judge whether or not the predetermined condition is satisfied in response to an event that the address value held in said first register for designating amount of delay is in agreement with a value of the program counter and starts to execute the operation designated by the second operation instruction when the predetermined condition is satisfied in response to an event that the address value held in said second register for designating amount of delay is in agreement with the value of the program counter.

9. A data processing device according to Claim 1, wherein

the instruction decoder decodes a third instruction among the plurality of instructions in a seventh period which is started after said third period, in order-to output a third control signal;

the instruction execution unit executes an operation designated by said third instruction in accordance with said third control signal and writes a result of the operation in a predetermined memory location in an eighth period which is started after said seventh period;

said second instruction designates an operation to be executed in a case that the operation result of said third operation instruction has a predetermined value; and

said instruction execution unit determines whether or not the operation designated by said second instruction is executed in reference of the predetermined memory location so that the starting of said fourth period is at least later than said eighth period.

10. A data processing device according to Claim 9, wherein

the predetermined memory location is a flag or a register; and

said third instruction is a comparison instruction which compares values of two registers and writes a result of the comparison in the predetermined memory location.

11. A data processing device according to Claim 1, wherein

the second operation instruction is a branch instruction, a jump instruction or an add instruction.

12. A data processing device according to Claim 1, wherein

each of the plurality of instructions has a field for designating an operation which designate contents of the operation, a field for designating a condition which designates an execution condition of the operation and a field for designating amount of delay which designates an amount by which timing for judging the execution conditions is delayed;

said first instruction is an instruction that is unconditionally executed and a description indicating an unconditionality is described in said field for designating the condition of said first instruction;

a description indicating a condition and a description indicating an interval between the ending or said third period and the starting of said fourth period are described respectively in said fields for designating the condition and the amount of delay of said second instruction;

the instruction decoder outputs the first control signal in accordance with said field for designating the operation of said first instruction and controls the instruction execution unit so that the instruction execution unit executes unconditionally the operation designated by said first instruction in said second period based on said field for designating the condition of said first instruction; and

the instruction decoder outputs said second control signal in accordance with said field for designating the operation of said second instruction, controls the instruction execution unit so as to judge whether or not the condition is satisfied in said fourth period in accordance with said field for designating the amount of delay and controls the instruction execution unit so as to determine whether or not the condition is satisfied in accordance with said field for designating the condition of said second instruction.

13. A data processing device according to Claim 1, wherein each of the plurality of instructions has a field for designating an operation which designates the contents of the operation, a field for designating a condition which designates the execution condition of the operation and a field for designating an amount of delay which designates the amount by which timing for judging the execution condition is delayed;

said first instruction is a conditional instruction;

a description indicating a first condition different from a second condition which is the predetermined condition of said second instruction is described in said field for designating the condition and a description indicating that said first condition should be judged in said first period is described in said field for designating the amount of delay respectively of said first instruction;

a description indicating said second condition is described in said field for designating the condition and a description indicating the interval between the ending of said third period and the starting of said fourth period is described in said field for designating the amount of delay respectively of said second instruction;

the instruction decoder outputs said first control signal in accordance with said field for designating the operation of said first instruction and controls said instruction execution unit so as to execute the operation designated by said first instruction based on said field for designating the condition and said field for designating the amount of delay of said first instruction in said second period;

said instruction decoder outputs said second control signal in accordance with the field for designating the operation of said second instruction, controls said instruction execution unit so as to judge whether or not said second condition is satisfied in accordance

with said field for designating the amount of delay of second instruction in said fourth period, and controls said instruction execution unit so as to determine whether or not said second condition is satisfied in accordance with said field for the condition of said second instruction.

14. A data processing device comprising:

an instruction decoder which sequentially decodes a plurality of instructions described in a program sequence and outputs a control signal corresponding to each instruction, and

an instruction execution unit which executes operations designated by the plurality of instructions in accordance with the control signals output from said instruction decoder, wherein

when one of said plurality of instructions is a conditional instruction for designating an operation to be executed under a condition, said instruction decoder outputs a first control signal by decoding said conditional instruction;

said instruction execution unit includes a first register for holding a first description indicating a timing for starting a determination of said condition; and

said instruction execution unit starts to determine whether or not said condition is satisfied in response to an event that the timing for starting the determination of the condition is detected based on said first description held in said first register, and starts to execute the operation designated by said conditional instruction in accordance with said first control signal and a result of the determination.

15. A data processing device according to Claim 14, wherein

said first description held in said first register can be variably set.

16. A data processing device according to Claim 14, further comprising:

a program counter which sequentially counts an address corresponding to each of the plurality of instructions and holds the address, wherein an address value is held in said first register as said first description; and

said instruction execution unit, detects an event that the address value held in said first register is in agreement with an address of said program counter and starts to determine whether or not said condition is satisfied in response to the detection.

17. A data processing device according to Claim 25, wherein

said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating condition which designates the executing condition of the operation and a field for designating an amount of delay which designate a timing for determining the execution condition;

said instruction decoder produces said first control signal based on contents described in said field for designating operation, outputs the second description in accordance with the contents described in said field for designating the condition and outputs the contents described in said field for designating the amount of delay;

said second description output from said instruction decoder is held in said third register; and

said instruction execution unit writes said first description in said first register in accordance with said field for designating the amount of delay output from said instruction decoder.

18. A data processing device according to Claim 14, wherein

the instruction execution unit further has a second register for holding a second description indicating a timing for starting the operation designated by the instruction; and

said instruction execution unit detects the timing for starting the operation designated by the instruction, determines whether or not the condition is satisfied in response to a result of the detection and starts the operation designated by the instruction in response to a result of the determination, in accordance with said second description.

19. A data processing device according to Claim 18, further comprising:

a program counter for sequentially counting an address corresponding to each of the plurality of instructions and holds the address, wherein

an address value is held in said first register as said first description;

an address value is held in said second register as said second description;

said instruction execution unit detects an event that the address value held in said first register is in agreement with an address of said program counter, starts to determine whether or not the condition is satisfied in response to the detection, detects an event that the address value held in said second register is in agreement with the address of said program counter and starts to execute the operation designated by said instruction in response to the detection.

20. A data processing device according to Claim 18, wherein

said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating a condition for designating an execution condition of the operation, a field for designating an amount of a first delay which designates a timing for determining the execution condition and a field for designating an amount of a second delay which designates a timing for starting the execution of the operation;

said instruction decoder produces said first control signal based on the contents described in said field for designating an operation, outputs the second description in accordance with the contents described in said field for designating a condition, and outputs the contents described in said field for designating an amount of said first delay and said field for designating an amount of said second delay, the second description output from said instruction decoder is held in said second register;

said instruction execution unit writes said first description in said first register in accordance with the contents described in said field for designating the amount of said first delay output from said instruction decoder and further writes said second description in said second register in accordance with the contents described in said field for designating the amount of said second delay output from said instruction decoder; and

said instruction execution unit further includes a third register for holding said first control signal output from said instruction decoder and a fourth register for holding a third description indicating the condition, said instruction execution unit performing the determination based on the third description held in said fourth register, reading the first control signal from said third register in response to the result of the determination, and

executing the operation in accordance with the first control signal read from said third register.

21. A data processing device comprising:

an instruction decoder decoding a condition instruction to output a control signal, said condition instruction specifying an operation to be executed under a condition and including a field specifying a timing of starting a determination whether the condition is satisfied; and

an instruction execution unit starting a determination of the condition on the basis of the field of said condition instruction and executing the operation under a result of the determination.

22. The data processing device according to claim 21, further comprising:

a program counter for calculating and outputting an address specifying an instruction to be fetched, wherein

said instruction execution unit includes a register into which a program counter value is written in accordance with the field of said condition instruction and starts the determination when detecting a coincidence of the program counter value held in said register with an address of said program counter.

23. The data processing device according to claim 22, wherein

said condition instruction includes another field specifying a timing of starting the operation, said instruction execution unit including another register into which a program

counter value is written in accordance with the other field of the condition instruction and starting to execute the operation when detecting a coincidence of the program counter value held in the other register with an address of said program counter.

24. The data processing device according to claim 21, wherein

said condition instruction includes another field specifying a timing of starting the operation, said instruction execution unit starting to execute the operation on the basis of the other field of the condition instruction.

25. The data processing device according to claim 14, wherein said instruction execution unit further includes a second register for holding said first control signal output from said instruction decoder and a third register for holding a second description indicating the condition,

said instruction execution unit performing the determination based on the second description held in said third register, reading the first control signal from said second register in response to the result of the determination, and executing the operation in accordance with the first control signal read from said second register.

APPENDIX B

Figs. 1, 2, 3, 8 and 9

FIGURE 1

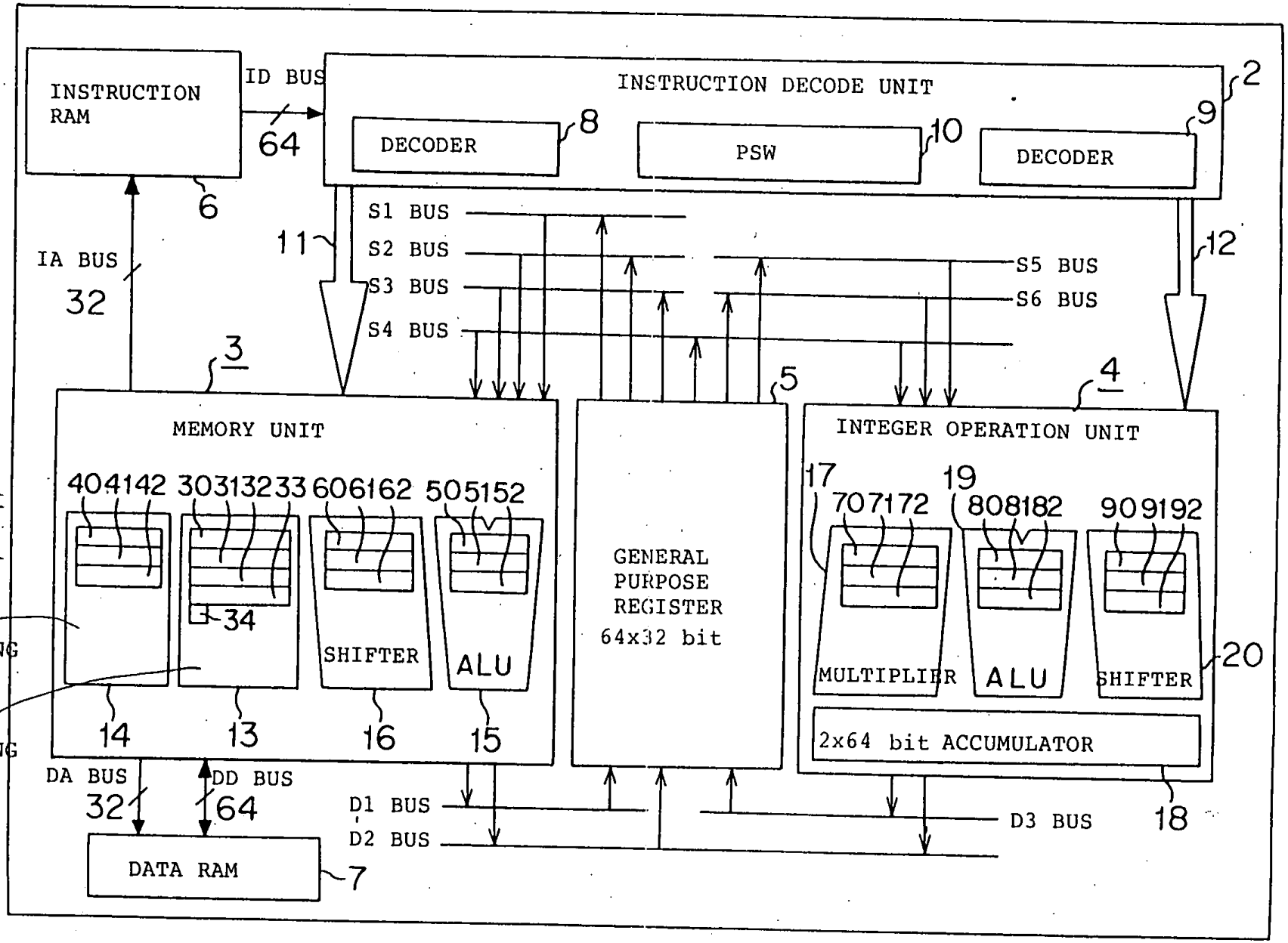
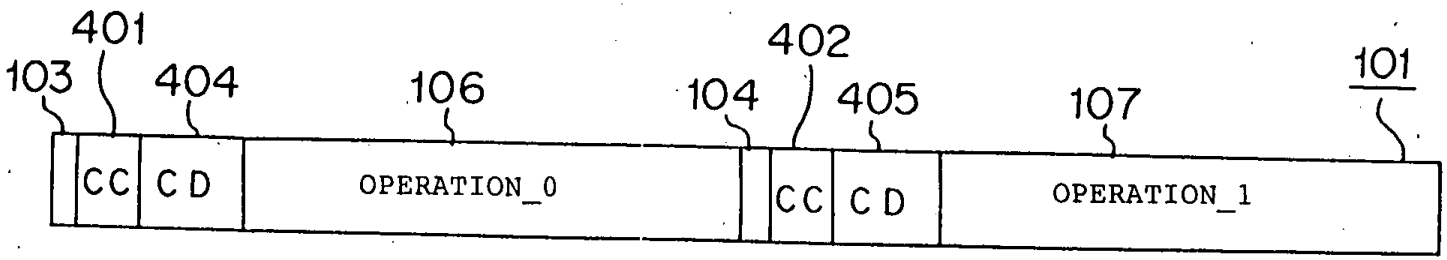

INSTRUCTION RAM
ID BUS
64
6
INSTRUCTION DECODE UNIT
2
DECODER
8
PSW
10
DECODER
9
11
12
S1 BUS
S2 BUS
S3 BUS
S4 BUS
S5 BUS
S6 BUS
IA BUS
32
3
5
4
MEMORY UNIT
INTEGER OPERATION UNIT
404142 30313233 606162 505152
707172 808182 909192
17
19
GENERAL PURPOSE REGISTER 64x32 bit
34
SHIFTER
ALU
MULTIPLIER
ALU
SHIFTER
20
MEMORY CONTROLLING PART
PC CONTROLLING PART
14
13
16
15
2x64 bit ACCUMULATOR
DA BUS
32
DD BUS
64
D1 BUS
D2 BUS
D3 BUS
18
DATA RAM
7

FIGURE 2 (a)



FM0 FM1

FIGURE 2 (b)

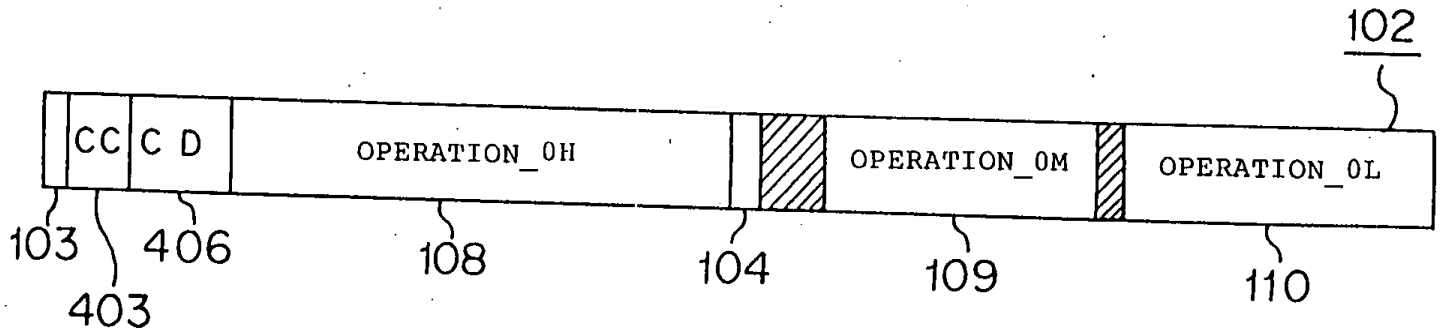
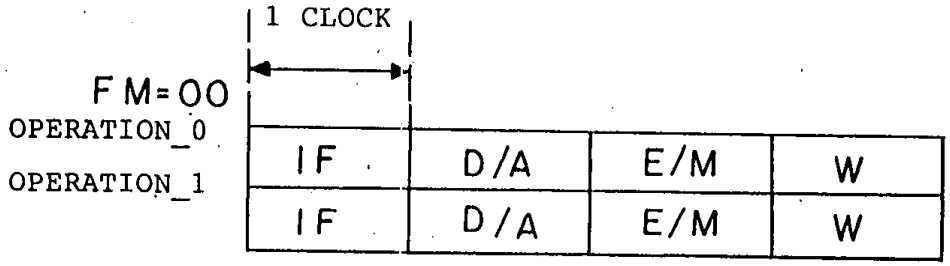
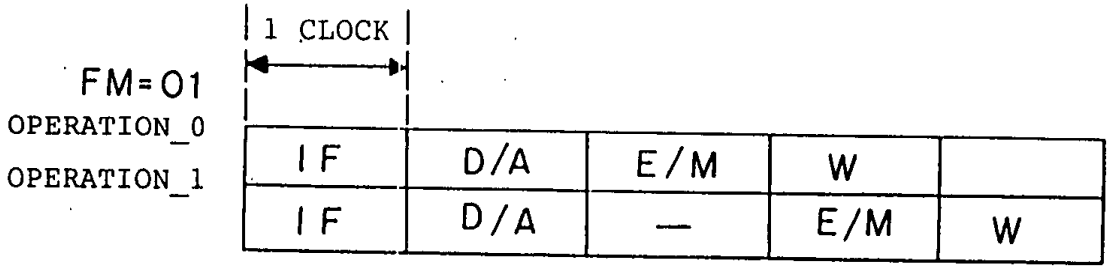


FIGURE 3 (a)



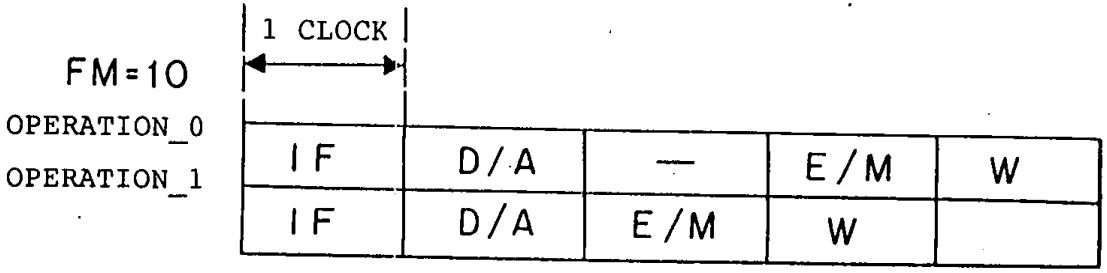
(a)

FIGURE 3 (b)



(b)

FIGURE 3 (c)

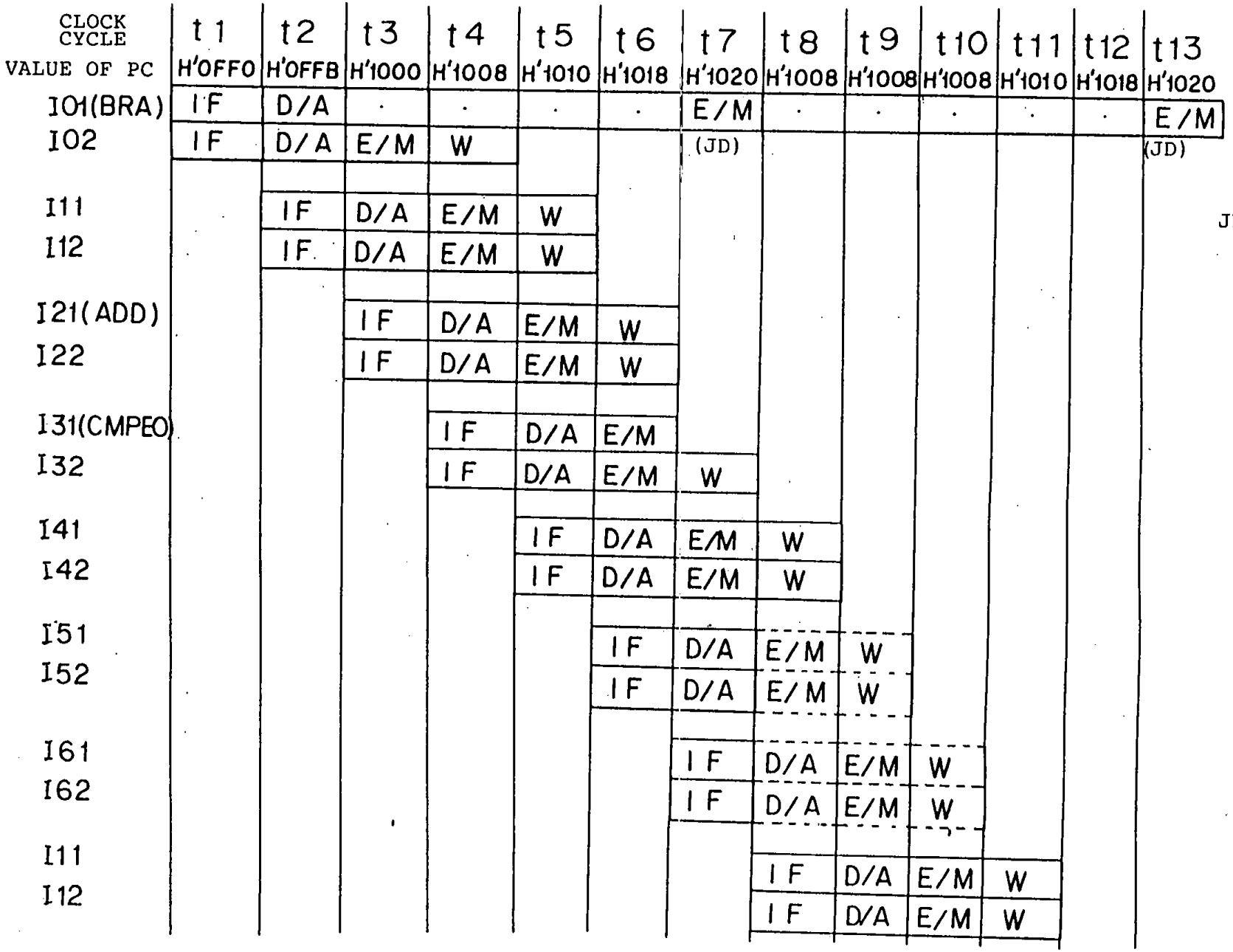


(c)

FIGURE 8

INSTRUCTION ADDRESS		OPERATION_0	OPERATION_1
H' 1000		I01 (BRA FOF # H' 20 loop)	I02:
H' 1008	loop:	I11	I12:
H' 1010		I21 (ADD R2,R2,R3)	I22:
H' 1018		I31 (CMPEO R2,R4,F0)	I32:
H' 1020	end:	I41	I42:
H' 1028		I51	I52:
H' 1030		I61	I62:

FIGURE 9


CLOCK CYCLE
VALUE OF PC
t1 H'0FF0
t2 H'0FF8
t3 H'1000
t4 H'1008
t5 H'1010
t6 H'1018
t7 H'1020
t8 H'1008
t9 H'1008
t10 H'1008
t11 H'1010
t12 H'1018
t13 H'1020
I01(BRA)
I02
I11
I12
I21(ADD)
I22
I31(CMPEQ)
I32
I41
I42
I51
I52
I61
I62
I11
I12
IF
D/A
E/M
W
(JD)
JD: JUDGING CONDITION